

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 61-030821
(43)Date of publication of application : 13.02.1986

(51)Int.Cl. H04B 1/10

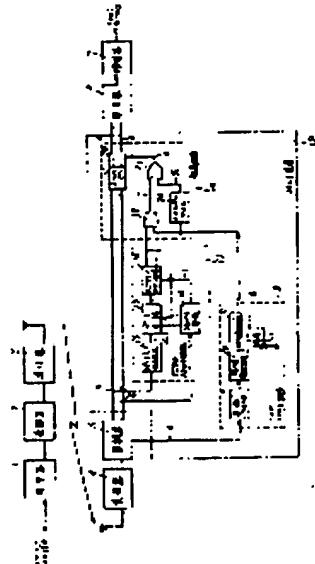
(21)Application number : 59-153528 (71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(22)Date of filing : 24.07.1984 (72)Inventor : IIZUKA SHOGO
TOMABECHI AKITAKA
YAMADA JUN

(54) SQUELCH DEVICE

(57)Abstract:

PURPOSE: To prevent decoding of a interference wave signal by providing a noise squelch circuit operated while detecting an out-band component of a demodulation signal and a digital squelch circuit operated while detecting a digital signal of a demodulation signal.

CONSTITUTION: A radio wave from a transmitter 3 is received by a receiver 4 and a demodulated signal (a) from a demodulator 5 and a bit synchronizing signal formed automatically from the signal (a) are transmitted to a squelch device 12. A noise squelch circuit 8 extracts the out-band component in the signal (a) and when the level is higher than a reference value, the circuit outputs ON and when lower, the circuit outputs OFF. On the other hand, a digital squelch circuit 13 detects whether or not a digital signal is a correct form from a bit synchronizing signal (b) and the signal (a) from the demodulator 5. Then an output of the circuits 8 and 13 is inputted to an accessory circuit 14 to control a squelch gate 22.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]